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ABSTRACT

We systematically investigate threshold voltage (V_{th}) instability in vertical GaN trench MOSFETs on sapphire using a charge pumping (CP) method combined with pulsed gate measurements. A negative V_{th} shift and reduced hysteresis are observed when switching the gate bias from DC to pulsed mode with a negative quiescent gate bias; this behavior is attributed directly to oxide trapping in the gate stack. Using the CP technique, we quantitatively extract the trap density, energy levels, and depth profiles of both border oxide traps and interface states in the Al_2O_3/p-GaN sidewall gate stack. An integrated border trap density of 7.28×10^{12} cm^{-2} is deduced, and amorphous Ga–O–Al bonds formed during atomic layer deposition are identified as the potential physical origin of the V_{th} shift and hysteresis (ΔV_{th}). Our analysis demonstrates that the CP approach goes beyond offering valuable insights into interface properties; it provides a powerful, quantitative diagnostic tool to directly guide the optimization of gate dielectrics in next-generation reliable vertical GaN trench MOSFETs for power applications.

Gallium nitride (GaN) is widely regarded as a key enabler for next-generation high-power electronics.[1] While lateral GaN high electron mobility transistors (HEMTs) have achieved widespread commercial adoption, vertical GaN trench MOSFETs continue to attract considerable research interest due to their potential for superior power handling and area-effective scaling.[2] By achieving higher breakdown voltage via a thicker drift layer, alongside avalanche ruggedness and inherent normally off operation, they are highly suitable for fail-safe high-power applications. However, the commercial viability of these vertical architectures remains bottlenecked by threshold voltage (V_{th}) instability.[3] This instability is generally attributed to the traps located at the dielectric/GaN interface (interface traps), near the dielectric border (border traps), and inside the dielectric bulk (bulk traps).[4]

Despite extensive research on V_{th} instability in MOS capacitors,[4–6] planar MOSFETs,[7,8] and trench devices,[9–12] few studies provide methods to quantitatively distinguish between these trap types. Established capacitance-based methods, such as conductance method[13] and deep-level transient spectroscopy (DLTS),[14] are difficult to apply due to the complex geometry and parasitic elements of the trench MOS gate structure.

To bypass these geometric limitations, we apply the charge pumping (CP) method to the gate dielectric/p-GaN system.[15] Unlike conductance and DLTS, which rely on capacitance, CP analyzes the recombination current generated directly from the p-GaN body,[15,16] enabling the independent extraction of energy distributions and depth profiles[15,17,18] for both interface and oxide traps. In this Letter, we present the first application of CP to characterize trap states in vertical GaN trench MOSFETs. By correlating CP measurements with V_{th} instability under a negative quiescent gate bias (V_{GSQ}) in pulsed mode, we systematically isolate the depth distributions of the oxide traps. Our profiling links the physical origin of these defects to amorphous Ga–O–Al bonds formed during oxygen-based gate dielectric deposition.

The quasi-vertical GaN trench MOSFETs in this work were grown on a sapphire substrate by metal-organic chemical vapor deposition (MOCVD). As shown in Fig. 1, the epitaxial structure consists of a 1-μm i-GaN buffer layer, a 1-μm n^+-GaN layer (Si: 5×10^{18} cm^{-3}), a 2.5-μm n^--GaN layer (Si: 5×10^{16} cm^{-3}), a 400-nm p-GaN layer (Mg: 1.2×10^{19} cm^{-3}), a 180-nm n^+-GaN layer (Si: 5×10^{18} cm^{-3}), and a 20-nm n^{++}-GaN layer (Si: 1×10^{19} cm^{-3}). The gate stack comprises a 50-nm Al_2O_3 gate dielectric deposited at 300 °C by atomic layer deposition (ALD) and a sputtered Ti/Al gate metal stack. The devices under test (DUTs) feature a rectangular trench with a length of 4 μm and a width of 100 μm. More detailed fabrication steps are described in our previous work.[19] To facilitate CP measurements, DUTs with separated source and body electrode terminals were also fabricated on the same wafer.

Figure 2 compares the threshold voltage and hysteresis characteristics extracted from DC and pulsed gate measurements. The transfer characteristics were acquired at a drain bias (V_{DS}) of 0.5 V, with V_{th} extracted at a drain current density (I_{DS}) of 1 A/cm^2, and ΔV_{th} defined as the voltage shift between the reverse and forward sweeps. Under DC double-sweep conditions [Fig. 2(a)], the device exhibits a V_{th} of 4.7 V and a pronounced ΔV_{th} of 1 V. In contrast, pulsed gate operation ($V_{GSQ}=-5$ V, pulse width/period = 2 ms/500 ms) yields a lower V_{th} of 2.68 V and negligible hysteresis. During pulsed double-sweep measurements (V_{GS} range: 0–15 V), V_{th} exhibits a continuous negative shift as V_{GSQ} decreases [Fig. 2(b)] and a positive shift as the gate pulse width extends [Fig. 2(c)]. The measured ΔV_{th} stabilizes at 0.3 V for V_{GSQ} values between 0 V and −6 V, shifting to −0.2 V at a V_{GSQ} of −10 V. Concurrently, ΔV_{th} is maintained at 0.25 V across gate pulse widths ranging from 2 to 400 ms at a fixed $V_{GSQ}=-5$ V. Figure 2(d) illustrates the temperature dependence of V_{th} and ΔV_{th} under pulsed operation. Across the 25–150 °C thermal range, V_{th} decreases monotonically, whereas ΔV_{th} exhibits a non-monotonic trend, turning over after an initial increase.

To qualitatively explain the above observed V_{th} and ΔV_{th} behaviors, energy band diagrams of the MOS gate stack with the charging dynamics under positive and negative gate biases are illustrated in Fig. 3. We distinguish the traps inside the Al_2O_3/GaN MOS gate stack into three types based on the trap location of depth with respect to the GaN channel surface, namely interface traps, border traps, and bulk traps.[4] Interface traps are located in closest proximity to the GaN; they exhibit relatively shorter emission periods and are usually attributed to dangling bonds and structural defects. The other two categories—border traps and bulk traps, unified as oxide traps in the following—are oxide related defects located farther from the GaN interface. These traps generally possess longer emission times and are often attributed to the Ga–O–Al bonds formed during oxygen-based atomic layer deposition of Al_2O_3.[4]

Under positive gate bias, electrons at the inverted GaN surface are injected into the interface and oxide traps [Fig. 3(a)], leading to a net increase in negative charges in the gate stack, thus a positive V_{th} shift. As the number of net trapped electrons increases with positive gate stress time, the large ΔV_{th} observed in the double DC sweep [Fig. 2(a)] and the V_{th} increasing with gate pulse width [Fig. 2(c)] can

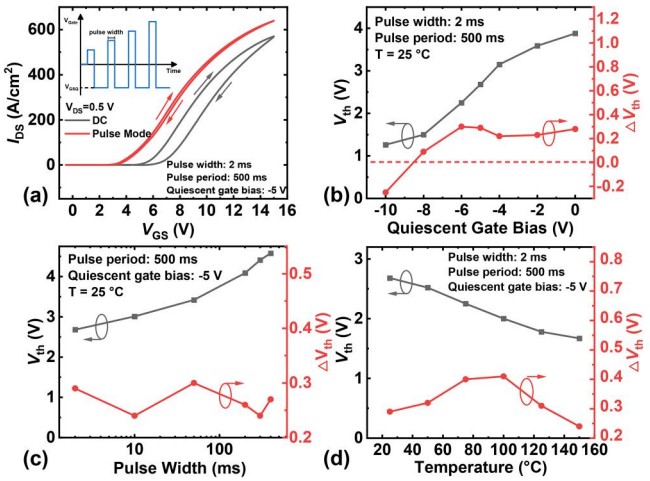

FIG. 2. (a) Comparison of transfer characteristics between pulsed and DC modes. V_{th} and ΔV_{th} (b) under different V_{GSQ} values with a pulse width/period of 2 ms/500 ms, (c) under different pulse widths with a fixed period of 500 ms and V_{GSQ} of −5 V, and (d) at varied temperatures under pulsed operation.

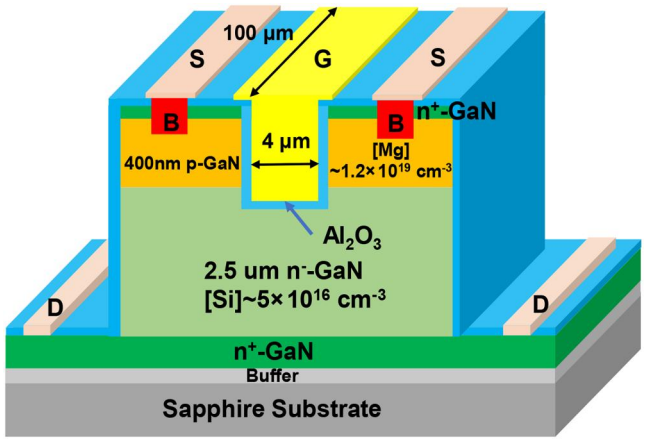

FIG. 1. 3D cross-sectional schematic of quasi-vertical GaN trench MOSFETs on sapphire.

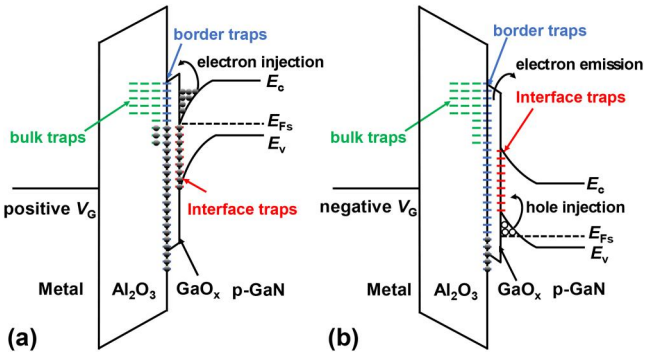

FIG. 3. Energy band diagrams of the MOS gate stack illustrating (a) the electron injection/trapping under positive gate biases and (b) electron emission and hole injection/trapping under negative gate biases. The GaO_x reflects Ga–O bonds of the GaN native oxide and Ga–O–Al bonds of the amorphous Al_2O_3 at the beginning of atomic layer deposition.

be easily understood. While during the negative quiescent gate bias stage of pulsed measurements, the reversed electric field in the MOS stack facilitates the emission of electrons initially captured by either oxide traps or interface states, as well as the injection of holes from the p-GaN body [Fig. 3(b)], resulting in a net reduction of negative charges in the gate stack and a potential net increase in positive charges. Both factors explain the negative shift of V_{th} in Fig. 2(a). As the decrease in V_{GSQ} increases the electric field strength in the gate, the number of net positive charges increases due to enhanced electron emission or hole injection, leading to a continuous negative shift of V_{th} shown in Fig. 2(b). With proper setting of V_{GSQ}, pulse width, and period in the pulsed operation, the dynamic charge trapping in the gate stack can be suppressed effectively, evidenced by the minimal ΔV_{th} in Fig. 2(a). Under this operation condition, the observed negative V_{th} shift with elevated temperature in Fig. 2(d) is mainly attributed to the increased intrinsic carrier concentration.[20] It can also be inferred that the dynamic charging in pulsed operation with a negative V_{GSQ} is the overall result of competition between electron trapping during the positive bias phase and the electron de-trapping, as well as hole trapping during the negative phase. When V_{GSQ} is ≥ -6 V, interface trap-density-limited electron trapping dominates the net increase in negative charges in the gate stack, resulting in a similar ΔV_{th} observed in Figs. 2(b) and 2(c). When the V_{GSQ} is < -6 V, hole injection starts to play an important role, which results in a net increase in positive charges in the gate stack. Consequently, the ΔV_{th} transitions from +0.3 V to −0.2 V as V_{GSQ} decreases from −6 to −10 V. The non-monotonic trend of ΔV_{th} at varied temperature can also be explained as the competition of electron trapping and emission: (i) for temperature below 100 °C, the increased thermal energy enhances the injection of electrons from the channel into the interface and oxide traps, but insufficient to release the electrons out of the traps, leading to aggravated ΔV_{th}; (ii) as temperature rises above 100 °C, the thermally activated de-trapping process becomes dominant, thus reducing the ΔV_{th}.

To quantitatively characterize oxide and interface traps and analyze their impact on the V_{th} instability, we employed the charge pumping method. Measurements were performed using a Keithley 4200A-SCS Parameter Analyzer equipped with a 4225-PMU Ultra-Fast I-V Module. During the CP measurements, a repetitive pulse was applied to the gate, while the source and drain were grounded; the body terminal was connected to a source measurement unit (SMU) to detect the CP current (I_{CP}). The experimental setup is illustrated in Fig. 4(a). The device features separated source and body electrode terminals, with a gate trench dimension of $4 \times 100\ \mu m^2$. For trap density extraction, the effective channel length is calculated using the 400-nm p-GaN thickness, accounting for the double sidewall MOS channels. We employed a constant base-level trapezoidal pulse with a 50% duty cycle, as shown in Fig. 4(b). In this waveform, V_{GL} and V_{GH} represent the low and high voltage levels, respectively, V_A denotes the pulse amplitude ($V_{GH} - V_{GL}$), and t_r and t_f correspond to the rise and fall times. When the gate is pulsed into inversion, electrons are captured by both interface and oxide traps within the gate stack. As the gate pulse is driving the p-GaN sidewall surface transitioning from inversion to accumulation, these trapped electrons recombine with holes, thereby contributing to the CP current.[15]

Figure 5 displays I_{CP} values under varied constant base-level pulsing. The black square curve represents the results measured in constant low-base-level mode with V_{GL} fixed at −10 V and V_{GH} swept from −10 to 15 V. The red circle curve represents the results measured in constant high-base-level mode with V_{GH} fixed at 15 V and V_{GL} swept from 15 V to −10 V. Both curves were measured at 10 kHz with pulse rise (t_r) and fall (t_f) times set to 5 μs. Geometric components in the I_{CP} are negligible, as the device has a large W/L ratio of 500.[21] According to Eq. (1), where q is the elementary charge, f is the frequency, A_{eff} is the effective channel area (p-GaN thickness times gate width with double side MOS channel, i.e., $2 \times 0.4 \times 100\ \mu m^2$), and N_{CP} is the trap density,

$$I_{CP}^{max} = qfA_{eff}N_{CP}, \tag{1}$$

N_{CP} is calculated to be $8.5 \times 10^{10}\ cm^{-2}$ from the constant low-base-level mode. From Fig. 5, we extract the V_{FB}^{CP} to be around −5 V and the V_{TH}^{CP} to be around 5 V. The V_{FB}^{CP} and V_{TH}^{CP} are related to the local carrier concentration ensuring steady-state capture (or emission) during the pulse phases, and also reflect the flatband voltage for channel accumulation and threshold voltage for channel inversion, respectively.[18]

Figure 6(a) shows the extracted N_{CP} from the frequency-dependent I_{CP}. Measurements were performed with a pulse rise/fall time of 5 μs, V_{GL} of −10 V, and V_{GH} of 15 V, while the frequency was swept from 50 kHz down to 5 Hz. As observed in Fig. 6(a), the trap density increases as the frequency decreases, eventually saturating between 5 and 20 Hz. The interface state density extracted at 50 kHz is approximately $2 \times 10^{10}\ cm^{-2}$, whereas the trap density in the saturation regime (5–20 Hz) reaches around $2 \times 10^{13}\ cm^{-2}$. This behavior is attributed to the increased contribution of deep-level traps at lower frequencies. Specifically, oxide traps become active around 10 Hz, leading to a significant rise in extracted trap density.[22]

The depth profile of these traps [$N_{ot}(x_m)$] can be derived from the frequency-dependent CP measurements using the following equation:[17]

$$N_{ot}(x_m) = -\frac{1}{q\lambda_n A_{eff}\Delta E_t}\frac{dQ_{CP}}{d\ln(f)}, \tag{2}$$

where λ_n is the tunneling attenuation coefficient, taken as 0.1 nm;[23] ΔE_t represents the energy range scanned by the electrons, determined by the rise and fall times (5 μs) of the trapezoidal pulse, corresponding to an energy range of $\Delta E_t = 2.68$ eV in this measurement;[18] and Q_{CP} is pumped charges per cycle, obtained from $Q_{CP} = I_{CP}/f$. To obtain the trap depth, x_m is derived using[17]

$$x_m = \lambda_n \ln\left(\frac{1}{2f}\sigma_n \nu_{th} n\right), \tag{3}$$

where σ_n is the capture cross section, assumed to be $10^{-15}\ cm^2$ in this test,[24,25] and n is the carrier density, defined as the effective acceptor concentration of $2 \times 10^{18}\ cm^{-3}$ extracted from the body bias effect.[26]

Figure 6(b) displays the depth profile of oxide traps in the Al_2O_3/GaN gate stack, extracted from the frequency-dependent CP current using Eqs. (2) and (3). The trap density N_{ot} initially increases and then decreases with the increase in depth, a trend similar to that observed in Si MOSFETs.[27] This profile reflects the coexistence of interface states and oxide traps. A relatively low interface state density is observed near the GaN surface; at a depth of 1.3 nm, N_{ot} is $8.8 \times 10^{17}\ cm^{-3}$

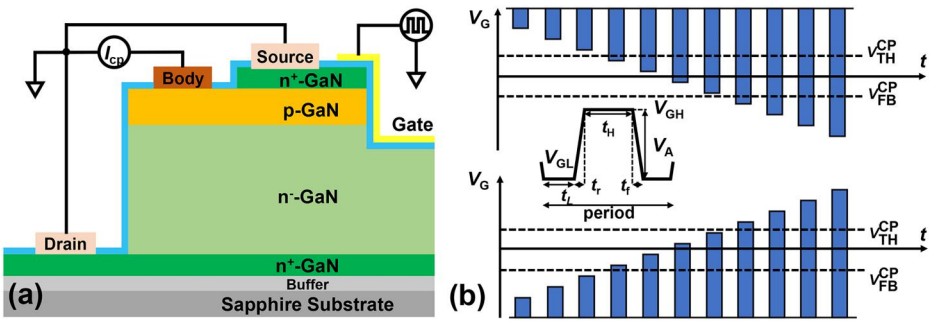

FIG. 4. (a) Experimental setup and (b) schematic sketch of the constant high-base-level gate pulses (top) and constant low-base-level gate pulses (bottom) of charge pumping measurements.

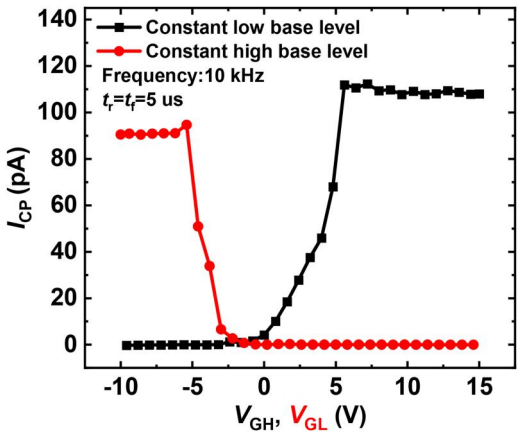

FIG. 5. CP currents for constant low-base-level gate pulses (black squares) and constant high-base-level gate pulses (red circles).

(corresponding to an areal density of $\sim 8.8 \times 10^{10}\,\mathrm{cm}^{-2}$). This low interface state density is attributed to the TMAH and piranha surface treatment, which effectively removes dry-etching-induced damage in the gate trench.[19,28] The initial increase in N_{ot} occurs because, during the early stages of ALD, the oxidant precursor may react with the GaN surface to form amorphous Ga–O–Al bonds.[29] This amorphous structure may act as oxide traps, causing the V_{th} shift. As the ALD process proceeds, the formation of Ga–O–Al bonds diminishes and high-quality Al_2O_3 is deposited, resulting in a decrease in N_{ot}. By integrating N_{ot} over the measured depth, we derive a total border trap density to be around $7.28 \times 10^{12}\,\mathrm{cm}^{-2}$, which is consistent with the value extracted from the frequency-dependent CP measurement. The oxide trapped electron state density associated with V_{th} shift in negative quiescent gate bias on pulse mode [Fig. 2(b)] can also be described as[4]

$$Q_{ot} = \frac{C_{ox}\left(V_{th}(\mathrm{DC,\ reverse-sweep}) - V_{th}(\mathrm{pulse,\ } V_{GSQ} = -5\,\mathrm{V})\right)}{qA}, \tag{4}$$

where Q_{ot} represents the trapped electron state density, C_{ox} is the accumulation capacitance, and V_{th} (DC, reverse-sweep) and V_{th} (pulse, $V_{GSQ} = -5$ V) are the V_{th} extracted from the reverse sweep under DC modes (5.7 V) and from the pulse mode with a -5 V V_{GSQ} (2.68 V), respectively [Fig. 2(a)]. This V_{th} difference was employed to quantify the overall trap density within the gate stack. This condition was selected because it represents the most severe electron trapping regime. Under DC reverse-sweep conditions, electron trapping is the dominant mechanism, leading to a maximum positive shift in the V_{th}. In contrast, under pulse modes with $V_{GSQ} = -5$ V, electron emission becomes dominant. As V_{GSQ} is lower than -5 V, hole injection may be triggered, thereby compromising the accuracy of the trap density characterization. From this V_{th} shift, an oxide trap state density Q_{ot} of $2.09 \times 10^{12}\,\mathrm{cm}^{-2}$ is extracted, which is approximately the same order of magnitude as that extracted by the frequency-dependent CP test of $7.28 \times 10^{12}\,\mathrm{cm}^{-2}$.

To extract the energy distribution of interface and border traps, we performed pulse fall-time-dependent CP measurements. Figure 7 shows the accessible energy range for GaN as a function of pulse fall time (t_f) and pulse rise time (t_r).[30,31] As t_f increases (with t_r fixed), the scanned energy range narrows, reducing the number of detected

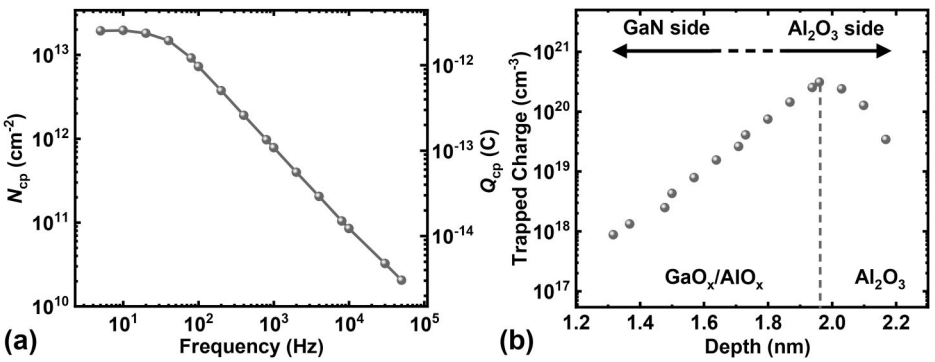

FIG. 6. (a) Interface states extracted from I_{CP} at different frequencies. (b) Depth profile of oxide traps in the Al_2O_3/GaN MOS stack extracted from frequency-dependent CP current.

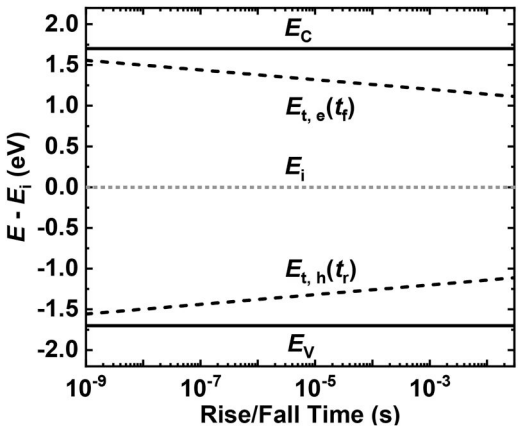

FIG. 7. Scannable energy level range for GaN as a function of the pulse fall time (t_f) and pulse rise time (t_r). Conduction band and valence band edges are shown as solid lines. Dashed lines represent scannable energy level edges of the hole traps and electron traps. The energy difference $|E_{t,\,e}(t_f) - E_{t,\,h}(t_r)|$ corresponds to the scanning energy range ΔE_t. $E_{t,\,e}(t_f)/E_{t,\,h}(t_r)$ defines the upper/lower limits of the measurable electron/hole trap energy levels with this t_r/t_f.

electron traps. By using a gate frequency below 100 Hz, we can determine the energy distribution of oxide traps, whereas higher gate frequencies allow for the characterization of interface traps.[15] Figure 8(a) plots the I_{CP} vs t_f from 25 to 175 °C at 1 kHz, and from 25 to 75 °C at 10 Hz, while Fig. 8(b) presents the corresponding extracted energy distributions. At 1 kHz between 25 and 175 °C, a broad interface state distribution is observed, with extracted energy levels spanning from 0.27 to 0.68 eV. The interface state density (D_{it}) rises from $\sim 1 \times 10^{12}$ to $6 \times 10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$, eventually stabilizing at $\sim 6 \times 10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$ at 175 °C. At 10 Hz, the border trap density is $\sim 10^{14}\,\mathrm{cm^{-2}\,eV^{-1}}$ and exhibits a decreasing trend with increasing temperature. For these border traps, at higher temperatures, carriers gain greater thermal energy and can occupy trap states located further into the gate dielectric. This spatial depth makes them less likely to return to the interface during the falling edge of the gate pulse, thus resulting in a decreased fall-time-dependent I_{CP} and D_{it} at elevated temperatures.[32]

For a more comprehensive trap characterization, D_{it} was additionally extracted via the temperature-dependent conductance method (Fig. 9). The device utilized for this characterization is a circular trench MOSFET with a diameter of 100 μm and a trench width of 4 μm. Figures 9(a) and 9(b) show the parallel conductance (G_p/ω) vs radial frequency (ω) for selected gate voltages near the threshold voltage at 25 and 175 °C, respectively. Figure 9(c) compares the D_{it} extracted via the conductance method with that obtained from the CP method. From the conductance method, an energy distribution of 0.21–0.43 eV was extracted over the temperature range of 25–175 °C. The D_{it} extracted from the conductance method ranges from 5.6×10^{12} to $8.2 \times 10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$, which is higher than the values obtained via the CP method. This expected discrepancy arises because the conductance method extracts the interface states from the entire trench interface, including the p-GaN layer, as well as from the overlapped n^+-GaN and n^--GaN regions, whereas the CP method is highly selective to the traps located specifically in the actively switched p-GaN channel region.

To contextualize these findings, Table I compares the room-temperature D_{it} values extracted from various Al_2O_3/GaN MOSCAP and trench MOSFET structures reported in the literature.[5,12,33–35] The reported D_{it} for these gate structures generally ranges from $\sim 1 \times 10^{12}$ to $2 \times 10^{13}\,\mathrm{cm^{-2}\,eV^{-1}}$. This demonstrates that the interface quality achieved in our work ($\sim 1 \times 10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$) is at a highly comparable and competitive level with recent state-of-the-art reports.

To mitigate the critical challenges posed by interface and border traps, several advanced processing strategies have been demonstrated in recent literature. For the suppression of interface traps, effective approaches include: (1) adopting alternative gate dielectric stacks, such as AlSiO,[36,37] AlON,[38] SiO_2,[39] or incorporating a thin AlN insertion layer.[40] With such gate stack modifications, the interface trap density has been successfully reduced to the order of $\sim 10^{11}\,\mathrm{cm^{-2}\,eV^{-1}}$; (2) performing appropriate pretreatment prior to gate stack deposition, such as buffered oxide etchant (BOE) cleaning and $(NH_4)_2S$ passivation;[4] and (3) applying post-deposition annealing (PDA) after gate dielectric deposition to heal interface defects.[41,42]

Similarly, several methods have been reported to successfully reduce border traps. One prominent approach utilizes NH_3/Ar/N_2 remote plasma treatments prior to gate stack deposition. In this process, NH_3/Ar is used to remove native oxide, while N_2 plasma passivates Ga dangling bonds, compensates for potential nitrogen vacancies (V_N), and facilitates the formation of a high-quality AlN interfacial layer.[43] Another reported method involves the deposition of a crystalline-like thin GaO_x layer via ALD prior to primary gate

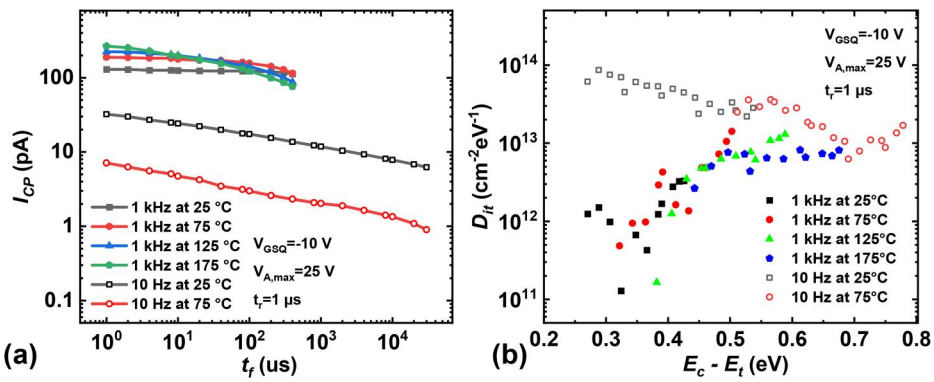

FIG. 8. (a) Temperature-dependent CP currents under varied pulse fall times at 10 Hz and 1 kHz and (b) extracted interface (1 kHz) and border trap (10 Hz) distributions.

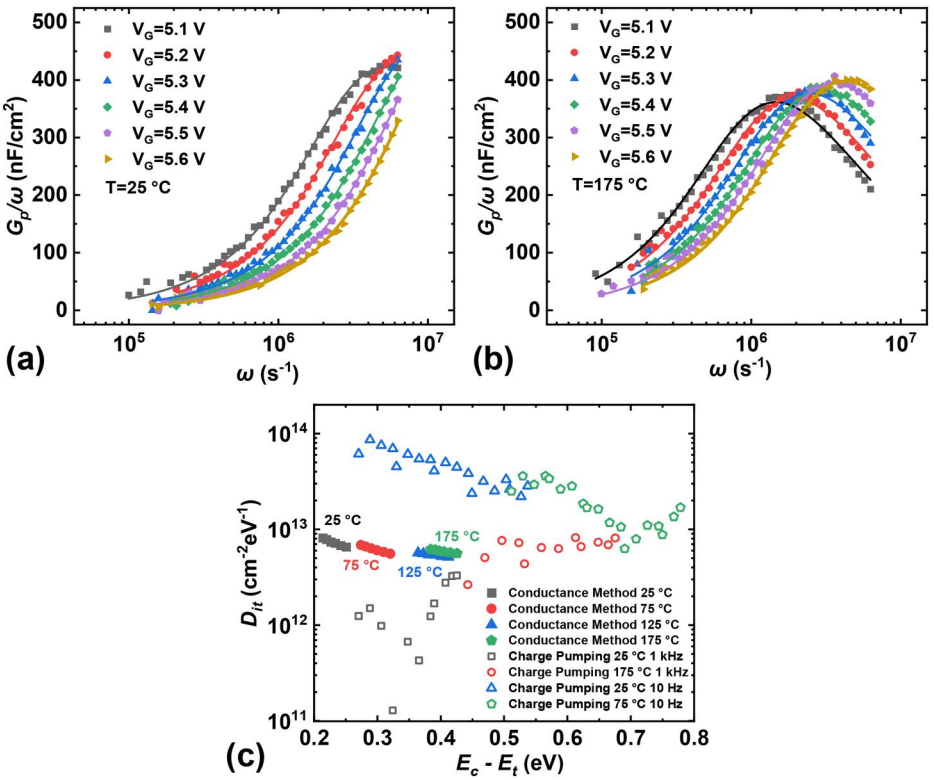

FIG. 9. Parallel conductance as a function of radial frequency under selected voltages at (a) 25 and (b) 175 °C. (c) Comparison of energy distributions extracted by conductance methods and by charge pumping methods.

TABLE I. Comparison of D_{it} values with other Al_2O_3/GaN gate structures.

Paper	Device	Substrate	Pretreatment	Al_2O_3 thickness (nm)	Density of interface states ($cm^{-2}eV^{-1}$)
Zhu *et al.*[33]	n-GaN MOSCAPs	GaN	$(NH_4)_2S$ and PEALD GaO_x	25	$\sim1\times10^{12}$ [w/o $(NH_4)_2S$ and GaO_x] $\sim8\times10^{10}$ [w/ $(NH_4)_2S$ and GaO_x]
Zagni *et al.*[5]	n-GaN MOSCAPs	Sapphire	NH_3 plasma	25	$\sim2\times10^{13}$
Taoka *et al.*[34]	n-GaN MOSCAPs	Sapphire	HCl	20	$\sim2\times10^{12}$
Sang *et al.*[35]	p-GaN MOSCAPs	Sapphire and GaN	$(NH_4)_2S$	20	$\sim7\times10^{12}$ (on sapphire) $\sim2\times10^{12}$ (on bulk GaN)
Mukherjee *et al.*[12]	Trench MOSFETs	Si	...	35	$\sim5\times10^{12}$
This work	Trench MOSFETs	Sapphire	Piranha and BOE	50	$\sim1\times10^{12}$

stack deposition, which effectively suppresses the border trap formation.[33]

In summary, this work presents the first application of the charge pumping method to quantitatively isolate both oxide traps and interface states in GaN trench MOSFETs. By employing frequency-dependent measurements, we have successfully extracted the density and depth profile of deep oxide traps (7.28×10^{12} cm^{-2}). The distinct spatial profile derived from this technique links the origin of the V_{th} shift to the formation of amorphous Ga–O–Al bonds during the initial atomic layer deposition of the oxygen-based gate dielectric. Furthermore, pulse fall-time-dependent CP measurements at elevated temperatures allowed for the precise extraction of a broad energy level distribution, distinguishing these slow-emitting border traps from the shallower interface states responsible for the observed DC hysteresis. A temperature-dependent conductance method is conducted to comprehensively characterize the interface traps. Ultimately, this work clarifies the physical origin of threshold voltage instability in GaN trench MOSFETs and establishes a powerful diagnostic tool to directly guide the optimization of gate dielectrics in next-generation high-power electronics.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Haowen Luo: Conceptualization (equal); Data curation (equal); Investigation (lead); Methodology (lead); Writing – original draft (lead). **Renqiang Zhu:** Conceptualization (equal); Methodology (equal); Validation (equal). **Xuancong Fan:** Data curation (equal); Writing – review & editing (equal). **Wen Yang:** Methodology (supporting); Writing – review & editing (supporting). **Kei May Lau:** Funding acquisition (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal). **Huaxing Jiang:** Funding acquisition (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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